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Semiconductor Group

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1265 BORREGAS AV
SUNNYVALE, CA. 9408

Device Name

JAN

Document Number

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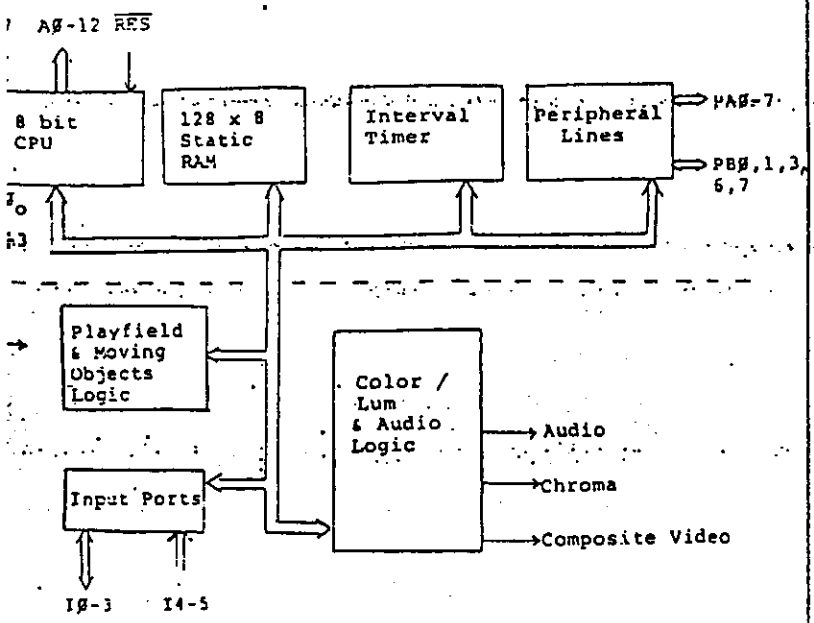
1. GENERAL DESCRIPTION

JAN is a 3u HMOS combination of the COMBO chip (6507 CPU; 6532 RAM, I/O, Timer) and the Stephanie chip (Television Interface Adapter). It consists of an 8 bit CPU, a 128 X 8 static RAM, two software-controlled bidirectional data ports with 8 and 5 bit interface between the chip and peripheral devices, and television interface capability. JAN is fully compatible with the 6502 instruction set.

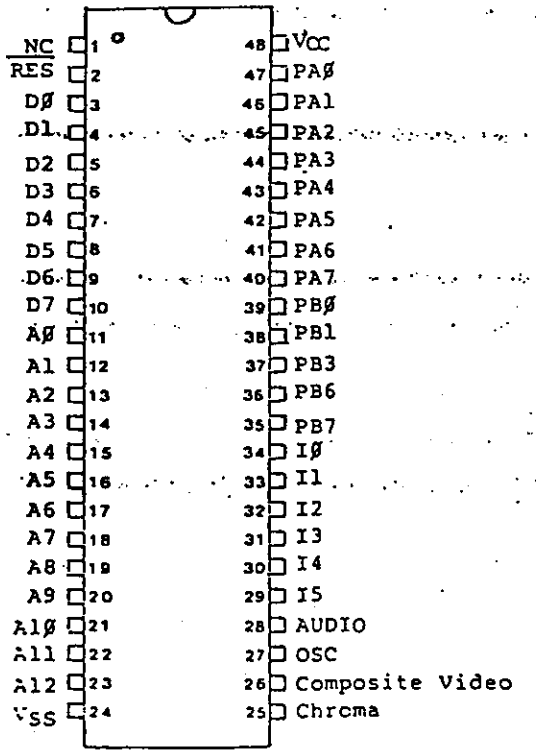
2. FEATURES

- o Cost reduction
- o Bidirectional 8 bit data bus
- o Direct memory access capability
- o Built in Schmitt Trigger for enhanced noise immunity for RESET
- o External clock input (3.58 MHz)
- o 128 X 8 static RAM
- o Two bidirectional data ports (8 and 5 bit)
- o Programmable interval timer
- o Single audio output
- o Internally combined luminance/sync lines for single composite video output
- o Color delay output

3. BLOCK DIAGRAM



4. PIN ASSIGNMENT



5. PIN DESCRIPTION

Pin Name	Type	Pin #	Function
V_{DD}	I	48	+5 volt supply.
V_{SS}	I	24	Ground.
$\overline{RES}$	I	2	Reset. When low, writing to or from JAN is inhibited. All 4 I/O registers will be zeroed. The I/O buses will act as inputs to protect external components from erroneous data or damage during system configuration.
D7-D0	I/O	10-3	Bidirectional, three-state data bus capable of driving one standard TTL load and 130 pF. D7 is the most significant bit.
A12-A0	I/O	23-11	TTL-compatible outputs capable of driving one standard TTL load and 130 pF. A12 is the most significant bit. The address bus can be used as an input during the testing mode.
PA7-PA0 PB7, PB6, PB3, PB1, PB0	I/O	40-47 35,36, 37,38, 39	Peripheral Data Ports. There are 2 peripheral I/O ports: Port A (8 lines) and Port B (5 lines). Each line is programmable as an input or an output. Writing a '0' to any bit position in the Data Direction registers (DDRA or DDRB) will program the corresponding line as an input. Writing a '1' to any bit position in the DDRA or DDRB will program the corresponding line as an output.
I0-I3	I/O	34-31	Dumped I/O ports with Schmitt trigger inputs and open drain outputs capable of driving 2 standard TTL loads and 10 pF.
I4-I5	I	30-29	Latched input ports with Schmitt trigger inputs and open source depletion pullup capable of driving 2 standard TTL loads and 10 pF.
OSC	I	27	3.58 MHz input clock with 50% duty cycle.
Composite Video	O	26	Composite Video. Made up of the luminance blanking, and sync lines.
Chroma	O	25	Color Clock. The color is determined by the delay time from the rising edge of the color clock.

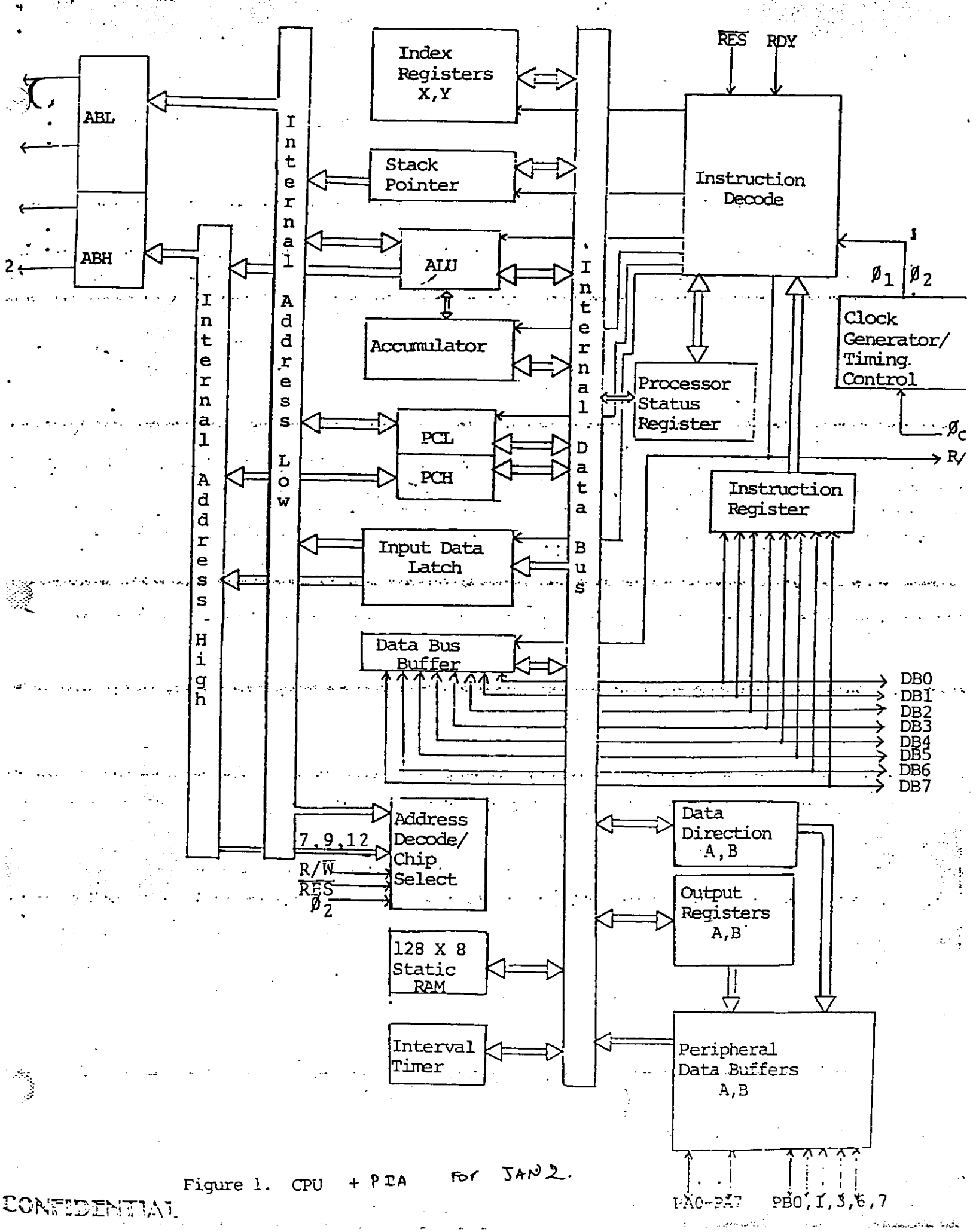


Figure 1. CPU + PIA for JAN 2.

Pin Description (cont.)

Pin Name	Type	Pin#	Function
Audio	O	28	Audio Output. The open drain audio channe has an internal frequency, noise and volume control.

6. FUNCTIONAL DESCRIPTION

6.1 CPU

The JAN CPU is a 6507 microprocessor with 8K addressable bytes of memory. The processor is clocked by a 1.19 MHz signal which is generated through a divide by 3 circuit whose input is the 3.58 MHz signal coming in through the OSC pin.

6.1.1 Reset Sequence

The power on reset sequence will begin when a positive edge is detected. RES must be held low for at least 2 clock cycles after Vcc reaches 4.75 volts during a power up sequence. After a system initialization time of 6 clock cycles, the mask interrupt flag will be set, and the processor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

6.1.3 Addressing Modes

Accumulator Addressing - This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

Immediate Addressing - The operand is contained in the second byte of the instruction with no further memory addressing required.

Absolute Addressing - The second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. The absolute addressing mode allows access to 65K bytes of addressable memory.

Zero Page Addressing - Allows for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte.

Indexed Zero Page Addressing - (X,Y indexing) - Used in conjunction with the index register and referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

Indexed Absolute Addressing - (X,Y indexing) - Used in conjunction with X and Y index register and referred to as "Absolute, X" and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

Implied Addressing - The address containing the operand is implicitly stated in the operation code of the instruction.

Relative Addressing - Used only with branch instructions and establishes a destination for the conditional branch. The second byte of the instruction becomes the operand which is an offset added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

Indexed Indirect Addressing - (referred to as (Indirect, X)) - The second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

Indirect Indexed Addressing - (referred to as (Indirect), Y)) - The second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

Absolute Indirect - The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

6.2 PIA SECTION

The PIA is a 6532 with 128 bytes of RAM, a programmable timer, and an 8 and 5 bit parallel I/O port.

6.2.1 PIA Addressing

Hex Address	Function	A9	A6	A5	A4	A3	A2	A1	A0	WR	RD
80	128 byte RAM	0	X	X	X	X	X	X	X	*	*
280	ORA	1	-	-	-	-	0	0	0	*	*
281	DDRA	1	-	-	-	-	0	0	1	*	
282	ORB	1	-	-	-	-	0	1	0	*	*
283	DDRB	1	-	-	-	-	0	1	1	*	
284	Read Timer	1	-	-	-	-	1	-	0		*
294	Timer, ÷ 1	1	-	-	1	-	1	0	0	*	
295	Timer, ÷ 8	1	-	-	1	-	1	0	1	*	
296	Timer, ÷ 64	1	-	-	1	-	1	1	0	*	
297	Timer, ÷ 1024	1	-	-	1	-	1	1	1	*	

X = Address - = Don't care * = Valid for WR/RD

TABLE 1. PIA Addressing Decode

.2.3 RAM

he 128 X 8 static RAM is internally addressed by A0-A6 (Byte Select), A7 CS1), A9 ($\overline{RS}$), and A12 ($\overline{CS2}$). The RAM is located in hex address range 80 hrough FF. The processor stack is located from FF down, and variables are ocated from 80 up.

.2.3 Interval Timer

ie Interval Timer contains a preliminary divide down register and a rogrammable 8 bit register as shown in Figure 2. The timer can be rogrammed to count up to 256 time intervals. Each interval can be either T, 8T, 64T or 1024T increments where T is the system clock period. When a ill count is reached, the internal clock continues counting down at a 1T ite to a maximum of -255T. This allows the user to read the counter and ien determine the total elapsed time. See Table 1 for addresses of iterval settings.

)r example, if the value 100 was written to hex address 296, the timer would crement to 0 in 6400 clocks (64 clocks per interval X 100 intervals) which also 6400 processor machine cycles. When the timer reaches 0, it holds ie zero count for one count time. Then the counter flips to FF hex and crements once each clock cycle. If a value of E4 is read from the timer ter interrupt, the time since interrupt will be 28T (the value read is the s complement).

Cont. PIA Section

The following calculations are used to compute the total time to interrupt and the total elapsed time:

Total time to interrupt = (Time Interval X Count) + 1

Total elapsed time = (Time Interval X Count) + Value Read After Interrupt

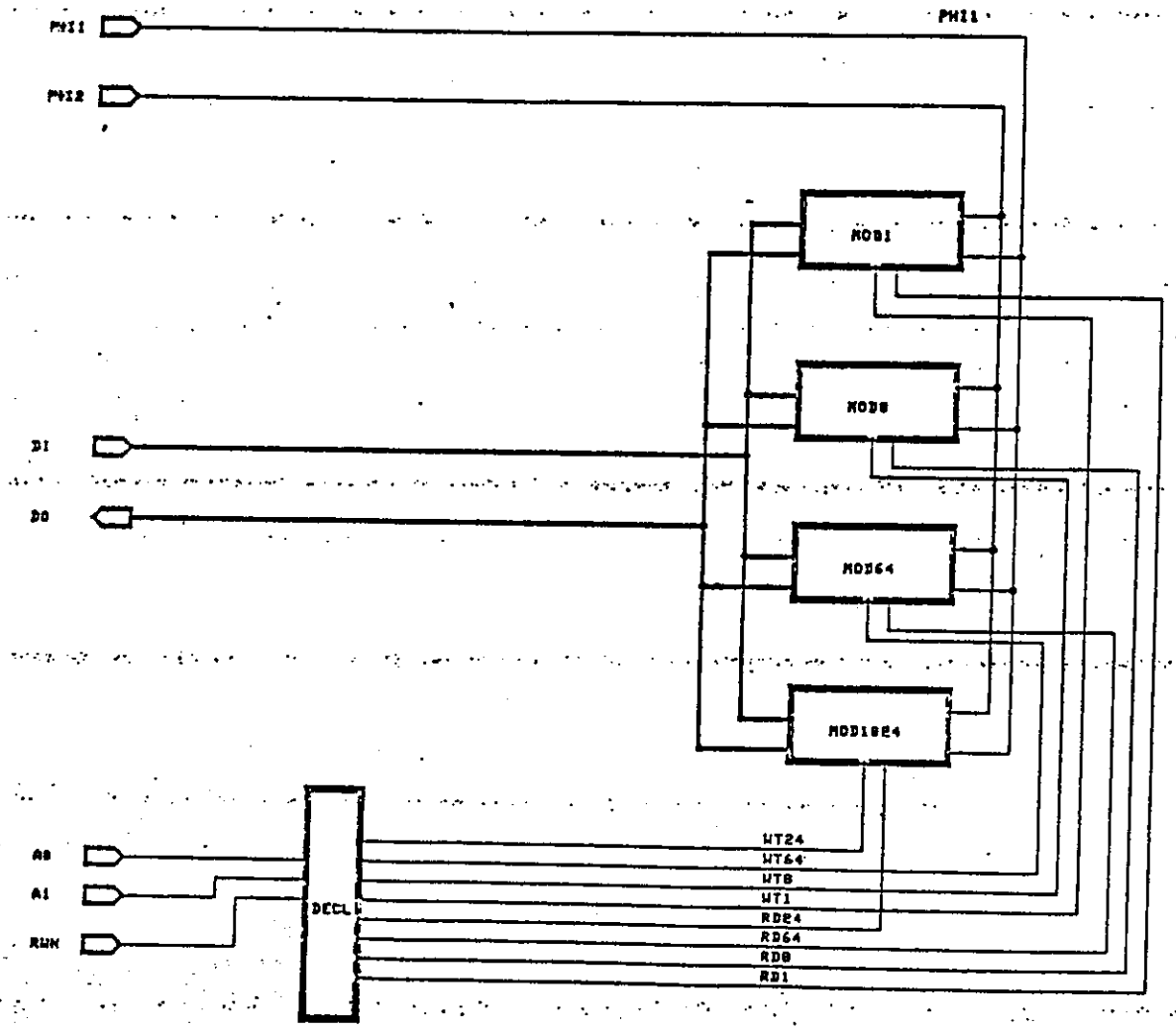


Figure 2. Interval Timer Circuit

6.2.4 Internal Peripheral Registers

There are four internal registers: 2 Data Direction registers and 2 Output registers. The A and B Data Direction registers (8 and 5 bits, respectively) control the direction of the data into and out of the peripheral I/O. A logic "0" in a bit of the Data Direction register (DDRA or DDRB) causes the corresponding line of the I/O port to act as an input. A logic "1" causes the corresponding line to act as an output. The voltage on any line programmed as an output is determined by the corresponding bit in the Output register (ORA or ORB).

Data is read directly from the PA lines during a peripheral read operation. For a PA pin programmed as an output, the data transferred into the processor will be the same as the data in the ORA only if the voltage on the line is allowed to be $\geq$ 2.4 volts for a logic "1" and $\leq$ 0.4 volts for a logic "0". If the loading on the line does not allow this, then the data resulting from the read operation may not match the contents of ORA.

The PB buffers are push-pull devices which are capable of sourcing 3 mA at 1.5 volts allowing these lines to directly drive transistor circuits. To assure that the processor will read the proper data when performing a peripheral read operation, logic is provided in the peripheral B port to permit the processor to read the contents of ORB, instead of the PB lines.

6.2.5 Peripheral I/O Ports

Port A is 8 bits wide, and Port B is 5 bits wide. Both ports can be set for either input or output. In the 2100 and 2600 game systems, Port A is used to interface to various hand-held controllers. Port B is dedicated to reading the status of the VCS console switches.

6.2.5.1 Port A

All 8 bits of Port A can be configured as an input or an output port through software control. It can be used to read or control various hand-held controllers with the data bits defined differently depending on the type of controller used.

6.2.5.1.1 Joystick Controllers

Two joysticks can be read by configuring the entire port as input and reading the data at address 280 hex according to the following table:

Data Bit	Direction	Player
D7	right	
D6	left	P0
D5	down	(left player)
D4	up	
D3	right	
D2	left	P1
D1	down	right player)
D0	up	

6.2.5.2 Port B

Port B is hardwired to be only an input port. The status of all the console switches is read from address 282 hex according to the following table:

Data Bit	Switch	Bit Meaning
D7	P1 difficulty	0 = amateur (B),1 = pro (A)
D6	P0 difficulty	"
D3	color - B/W	0 = B/W,1 = color
D1	game select	0 = switch pressed
D0	game select	0 = switch pressed

6.3 TELEVISION INTERFACE

6.3.1 SYNCHRONIZATION

6.3.1.1 Horizontal Timing

When the electron beam scans across the TV screen and reaches the right edge, it must be turned off and moved back to the left edge of the screen to begin the next scan line. This is taken care of by a hardware counter which produces all horizontal timing (sync, blank, burst, etc.) independent of the processor. The counter is driven from an external 3.58 MHz oscillator. It allows 160 color clocks (clock pulses) for the beam to reach the right edge, then generates a horizontal sync signal (HSYNC) to return the beam to the left edge. It also generates the signal to turn the beam off (horizontal blanking) during its return time of 68 color clocks (blank time). The total count across is 228 color clocks. Sync and color burst are decoded as 16 counts. See Figure 3 for TV frame set up.

6.3.1.2 Vertical Timing

When the electron beam has scanned 262 lines vertically, the TV set must be signalled to blank the beam and position it at the top of the screen to start a new frame. This signal is called vertical sync. Vertical sync must be transmitted for at least 3 scan lines. Writing a "1" to D1 of the VSYNC register turns on the vertical sync. Then at least 3 scan lines are counted. Writing a "0" to D1 of VSYNC turns the vertical sync off.

The processor is free to execute other software during the vertical blank and sync command times.

6.3.1.3 Microprocessor Synchronization

The microprocessor's clock is the 3.58 MHz oscillator divided by 3 or 1.19 MHz. One machine cycle is equivalent to 3 color clocks. One complete scan line of 228 color clocks results in 76 machine cycles per scan line. Since the software program loops and branches require different lengths of time to run, additional synchronization is needed between the software and the hardware. The synchronization problem is solved by the one bit latch called WSYNC (wait for sync). Writing to WSYNC causes the processor to halt until the electron beam reaches the right edge of the screen. Then, the processor resumes operation at the beginning of the 68 color clocks for horizontal blanking. When the WSYNC latch is set high, it drives the ready line (RDY), which is internally connected to the processor, low. A low on the RDY line causes the processor to halt and wait. WSYNC is automatically reset to zero by the leading edge of the next horizontal blank timing signal which then releases the RDY line and allows the processor to begin its computation and register writing for this horizontal line or line pair. See Figure 3 for timing.

6.3.1.4 Composite Sync

Horizontal and vertical sync are combined together to produce the composite sync. This composite sync signal and the luminance lines are fed through a DAC. The output of the DAC drives the external Composite Video output pad.

A "0" in a data bit indicates the joystick has been moved to close that switch. All "1"'s in a player's nibble indicates that joystick is not moving. The trigger button are read at INPT4 and INPT5.

6.2.5.1.2 Paddle Controllers

The 4 paddle trigger buttons can be read at address 280 hex according to the following table:

Data Bit	Paddle Number
D7	P0
D6	P1
D3	P2
D2	P3

A "0" in a data bit indicates the paddle trigger button has been pressed. The paddles themselves are read at INPT0 through INPT3.

6.2.5.1.3 Keyboard Controllers

The keyboard controller has 12 buttons arranged into 4 rows and 3 columns. A signal is sent to a row, then the columns are checked to see if a button is pushed, then the next row is signaled and all columns sensed, etc. until the entire keyboard is scanned and sensed. The PIA sends the signals to the rows, and the columns are sensed by reading INPT0, INPT1, and INPT4. With Port A configured as an output port, the data bits will send a signal to the keyboard controller rows according to the following table:

Data Bit	Keyboard Row	Player
D7	bottom	
D6	third	P0
D5	second	(left player)
D4	top	
D3	bottom	
D2	third	P1
D1	second	(right player)
D0	top	

** A delay of 400 microseconds is necessary between writing to the keyboard controller and reading the INPT ports.

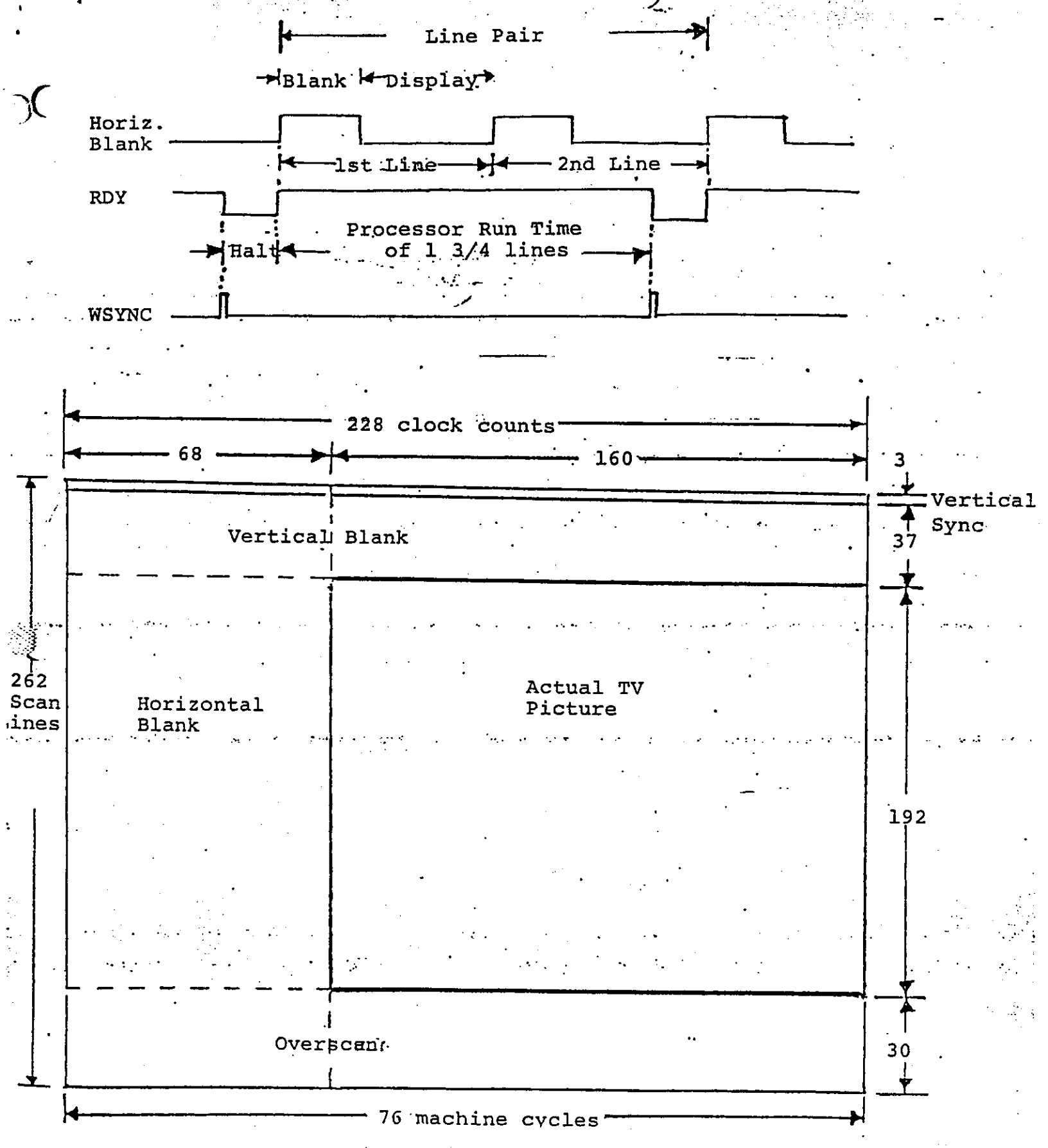


Figure 3 . TV Frame/WSYNC timing

6.3.2 PLAYFIELD

Objects which are not required to move are written into a 20 bit register called the Playfield Register. This low resolution register when written to draws the left half of the TV screen only. The right half of the screen is drawn by software selection of either a duplication or a reflection (mirror image) of the right half. The 20 bits are written into 3 addresses: PF0, PF1, and PF2. PF0 constructs the first 4 bits of the playfield, starting at the left edge of the TV screen. PF1 constructs the next 8 bits and PF2 the last 8 bits which end at the center of the screen. The PF register is scanned from left to right. The PF color is drawn wherever a "1" is found and the BK (background) color is drawn wherever a "0" is found. Zeroes must be written to all 20 bits of the playfield register to clear the playfield.

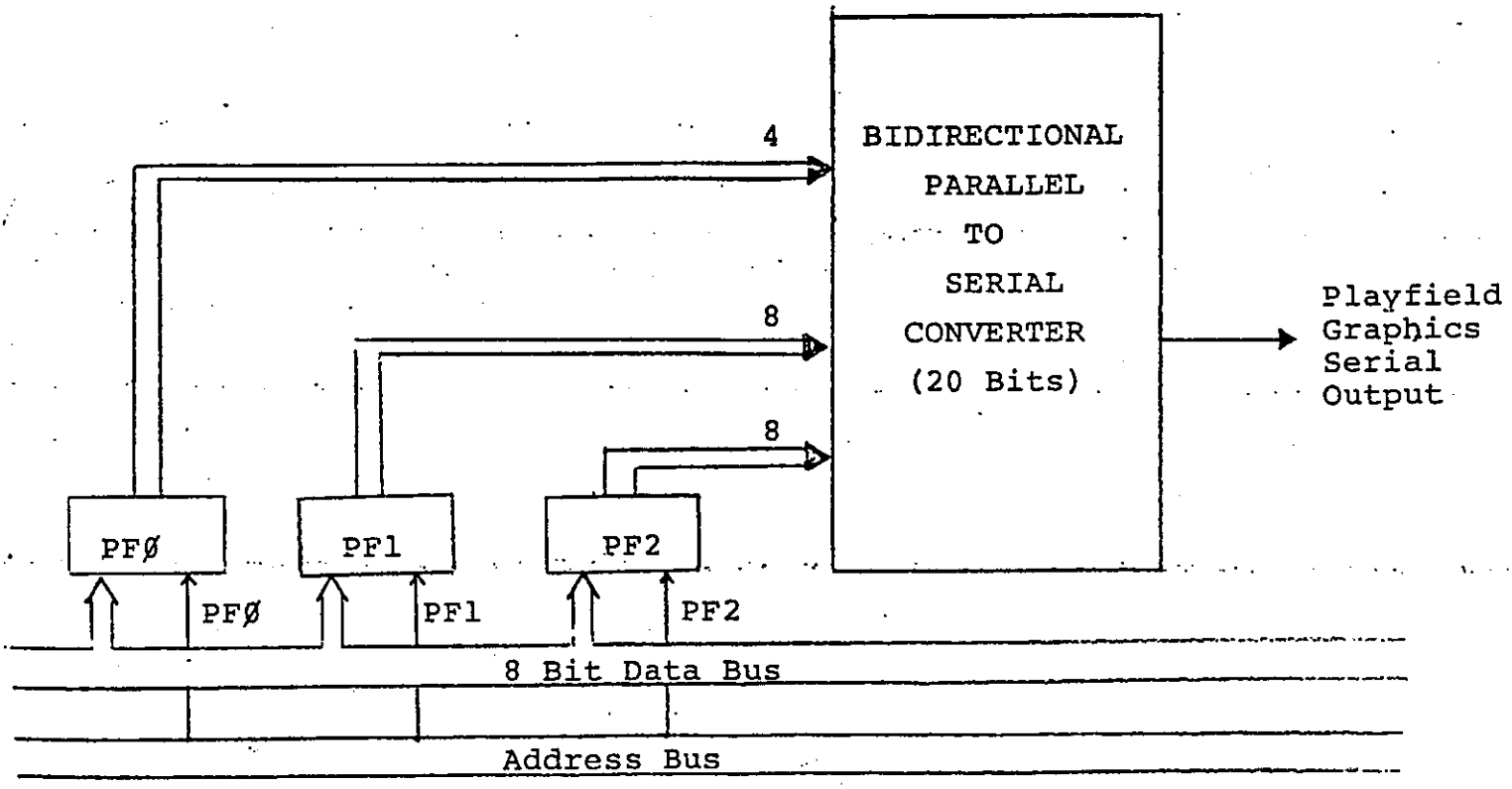
The playfield may be loaded at any time. It is a fixed graphics register, always starting its serial output when triggered by the beginning of each television line. Even though the playfield bytes (PF0, PF1, and PF2) may be written at any time, if one of them is changed while being serially scanned, part of the new value may show up on the television horizontal line. See Figure 4 for playfield circuit.

6.3.2.1 Normal Serial Output

The Playfield Register is automatically scanned and converted to serial output by a bi-directional shift register clocked at a rate which spreads the twenty bits out over the left half of a horizontal line. This scanning is initiated by the end of horizontal blank (left edge of TV screen). If a zero has been written to bit 0 of the Playfield Control Register (CTRLPF), the same scan will be repeated, duplicating the same twenty bit sequence over the right half of the horizontal line. See Section 7.3 for CTRLPF bit assignments.

6.3.2.2 Reflected Serial Output

A reflected playfield may be requested by writing a one into bit zero of the CTRLPF register. When bit zero is true the scanning shift register will scan the opposite direction during the right half of the horizontal line, reversing the twenty bit sequence.



PLAYFIELD GRAPHICS

Figure 4.

6.3.3 MOVEABLE OBJECTS GRAPHICS

All 5 moveable objects (P0, M0, P1, M1, and BL) can be assigned a horizontal location on the screen and moved left or right relative to that location. The vertical location is determined on whichever scan lines the objects graphics registers are enabled. The graphics registers are scanned when triggered by a start decode from their horizontal position counter and then converted to serial output. See Figure 6 for a typical graphics register.

6.3.3.1 Missile Graphics

The missile graphics registers consist of a one bit register called Missile Enable (ENAM0, ENAM1). Writing a "1" to the Missile Enable register will draw a missile on the scan line. Writing a "0" will disable the missile graphics. Each missile's left edge is positioned by a horizontal position register. The right edge is determined by the width of the missile. The missile width is assigned by writing into bits D4 and D5 of the Number-Size registers (NUSIZ0, NUSIZ1). This in effect extends the missile out over 1, 2, 4 or 8 color clock counts (one full scan line is 160 color clocks).

6.3.3.2 Ball Graphics

The ball graphics register (ENABL) consists of a single enable bit whose output is triggered by the ball position counter. It has two control bits (D4 and D5 of CTRLPF) that can extend the single graphics bit out over widths of 1, 2, 4 or 8 clocks of horizontal line time. The ball can also be vertically delayed one scan line by writing a "1" to D0 of the BL Vertical Delay register (VDELBL). The vertical delay capability was made available because most programs update the television interface adapter every 2 lines which confined all vertical movements of objects to 2 scan line jumps. The vertical delay allows the ball to move one scan line at a time.

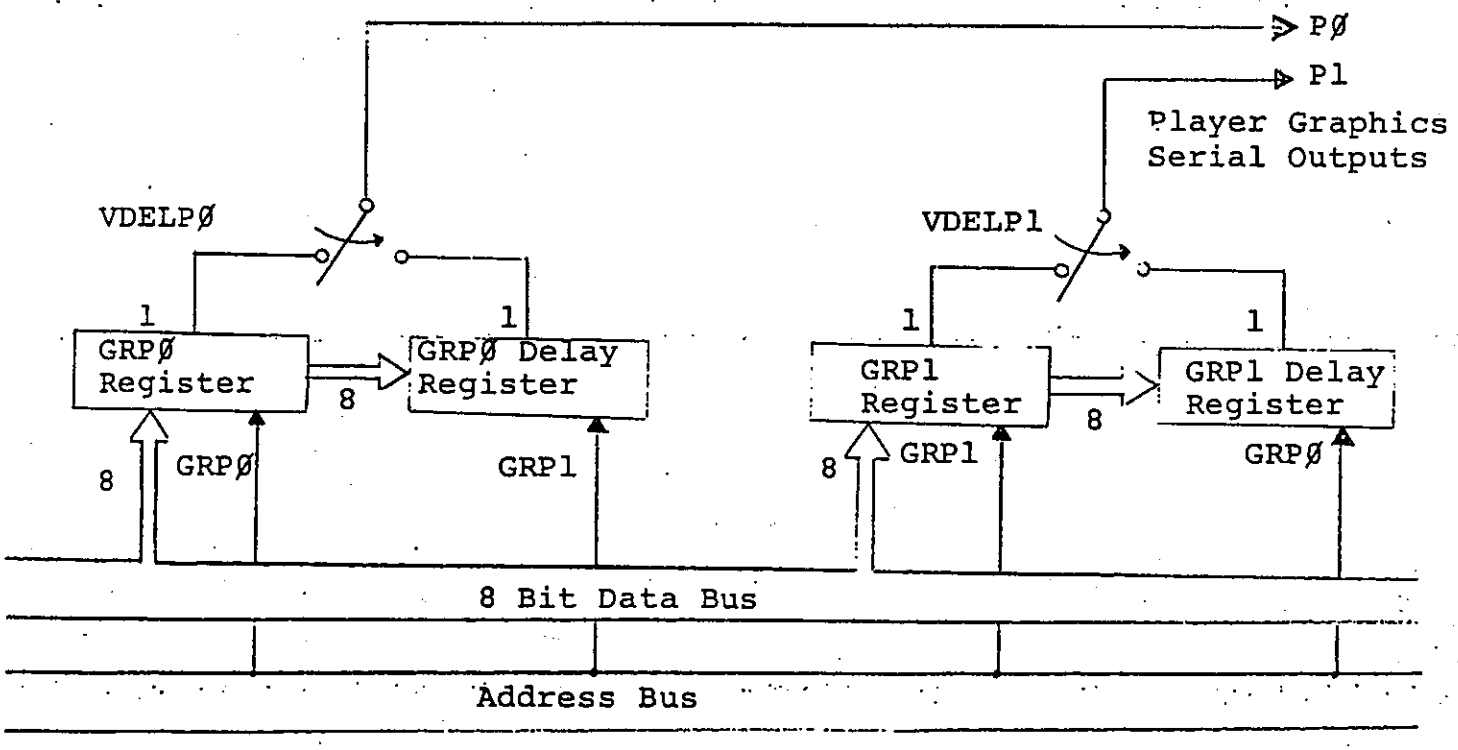
6.3.3.3 Player Graphics

There are actually two 8 bit parallel registers per player: GRP0, GRP0 delay and GRP1, GRP1 delay. The normal and delayed data are selectable by the Player Vertical Delay Control circuit (see Figure 5). The players are serially generated from the 8 bit graphics registers and are normally scanned from D7 to D0. The player color is drawn when the bit equals "1". If the bit equals "0", the background color is drawn. The scan direction of the serial player graphics registers is determined by D3 of the player reflection register (REFP0, REFP1). Writing a "1" to D3 reflects the graphics data with D0 at the left side of the player image. Writing a "0" to D3 restores the original image with D7 on the left side.

One can select from 1 to 3 copies of the player, spacing between those copies, and the size of the player by writing to bits D2 through D0 of the Number-Size registers (NUSIZ0, NUSIZ1). The players' widths can be 8, 16, or 32 color clocks wide (this is accomplished by slowing the scan rate by controlling the clock that goes into the scan counter).

6.3.3.3.1 Vertical Delay

The amount of processor time required to generate player, missile and playfield graphics and load registers is normally too large to be done in one horizontal line time. To solve the time problem, each player's graphics register is written to every two scan lines. The data is then serially output twice between writes. Vertical height resolution is limited to multiples of two lines. Vertical motion, however, can be resolved to a single scan line by writing alternately to GRP0 and GRP1 during the blank time just prior to each scan line. The GRP0 and GRP1 addresses from the processor alternate, so they are delayed by one line from each other. The GRP0 address decode can load the delayed graphics register for Player 1, and the GRP1 address decode can load the delayed graphics register for Player 0. Bit 0 of the Vertical Delay registers (VDEL0, VDEL1) selects which of the two registers (normal or delayed) will be used for serial output. If the vertical delay bit is set between picture frames, the player will be moved down (delayed) one line during the next frame.



Vertical Delay

Figure 5.

6.3.4 HORIZONTAL POSITION COUNTERS

The serial outputs of the five moveable objects are triggered by 5 separate horizontal position counters every time the counters pass through zero count. These postion counters are clocked continuously during the unblanked portion of every horizontal line and their count length is exactly equal to the normal number of clocks supplied to them during this time. They will pass through zero at the same time during each horizontal television line, and the triggered outputs will have no horizontal motion. See Figure 6 for a typical horizontal counter. Some position counters have extra decodes in addition to a zero decode to trigger multiple copies of the same object across a horizontal line.

All position counters can be reset to zero count by the processor at any time by a write instruction to the reset strobe addresses (RESBL, RESM0, RESM1, RESP0, RESP1). See Section 7.9. If reset occurs during horizontal blank, the object will appear at the left side of the television screen. Properly timed resets may position an object at any horizontal location consistent with the processor cycle time. For example, if the electron beam was 60 color clocks into a scan line when RESP0 was written to, player 0 would be positioned 60 color clocks 'in' on the next scan line.

It can take up to 5 machine cycles to write to a register. Since there are 3 color clocks per machine cycle, the programmer is confined to positioning the objects at 15 color clock intervals across the screen.

6.3.4.1 Ball Position Counter

The ball position counter has only the zero crossing decode and therefore cannot trigger multiple copies of the ball graphics.

6.3.4.2 Player Position Counters

Each player position counter has three decodes in addition to the zero crossing decode. These decodes are controlled by bits 0, 1, and 2 of the Number Size Control registers (NUSIZ0, NUSIZ1). They trigger 1, 2, or 3 copies of the players with different spacings across a horizontal line as shown in Section 7.4.2. These same control bits are used for the decodes on the missile position counter to insure an equal number of players and missiles.

6.3.4.3 Missile Position Counters

Missile position counters are identical to the player position counters except that they have another type of reset in addition to the previously discussed horizontal reset. Writing a "1" to D1 of the Reset Missile-to-Player register (RESMP0, RESMP1) disables that missile's graphics and repositions it horizontally to the center of its associated player. Until a "0" is written to the register, the missile's horizontal position is locked to the center of its player in preparation to be fired again.

6.3.5 HORIZONTAL MOTION

Five write only registers (HMP0, HMP1, HMM0, HMM1, HMBL) contain the horizontal motion values for each of the five moving objects. The motion values are written into Bits 4 through 7 of the Horizontal Motion Registers. These registers supply extra or fewer clocks to the horizontal position counters. This motion is not executed until the HMOVE register is written to, at which time all motion registers move their respective objects. Objects can then be be moved repeatedly by simply executing HMOVE.

The 4 bit long registers can be loaded with positive (left motion), negative (right motion), or zero (no motion) values. Negative values are represented in twos complement form. These registers are cleared to zero (no motion) simultaneously by an HMCLR command from the processor. They can also be cleared individually by loading zeroes into each register. See Section 7.6 for horizontal motion values.

The HMOVE command must immediately follow a WSYNC (wait for SYNC) to insure the HMOVE operation occurs during horizontal blanking. This insures that the HMOVE operation begins at the leading edge of horizontal blank and has the full blank time to supply extra or fewer clocks to the horizontal position counters. The 5 Horizontal Motion Registers should net be modified for at least 24 computer cycles after the HMOVE command.

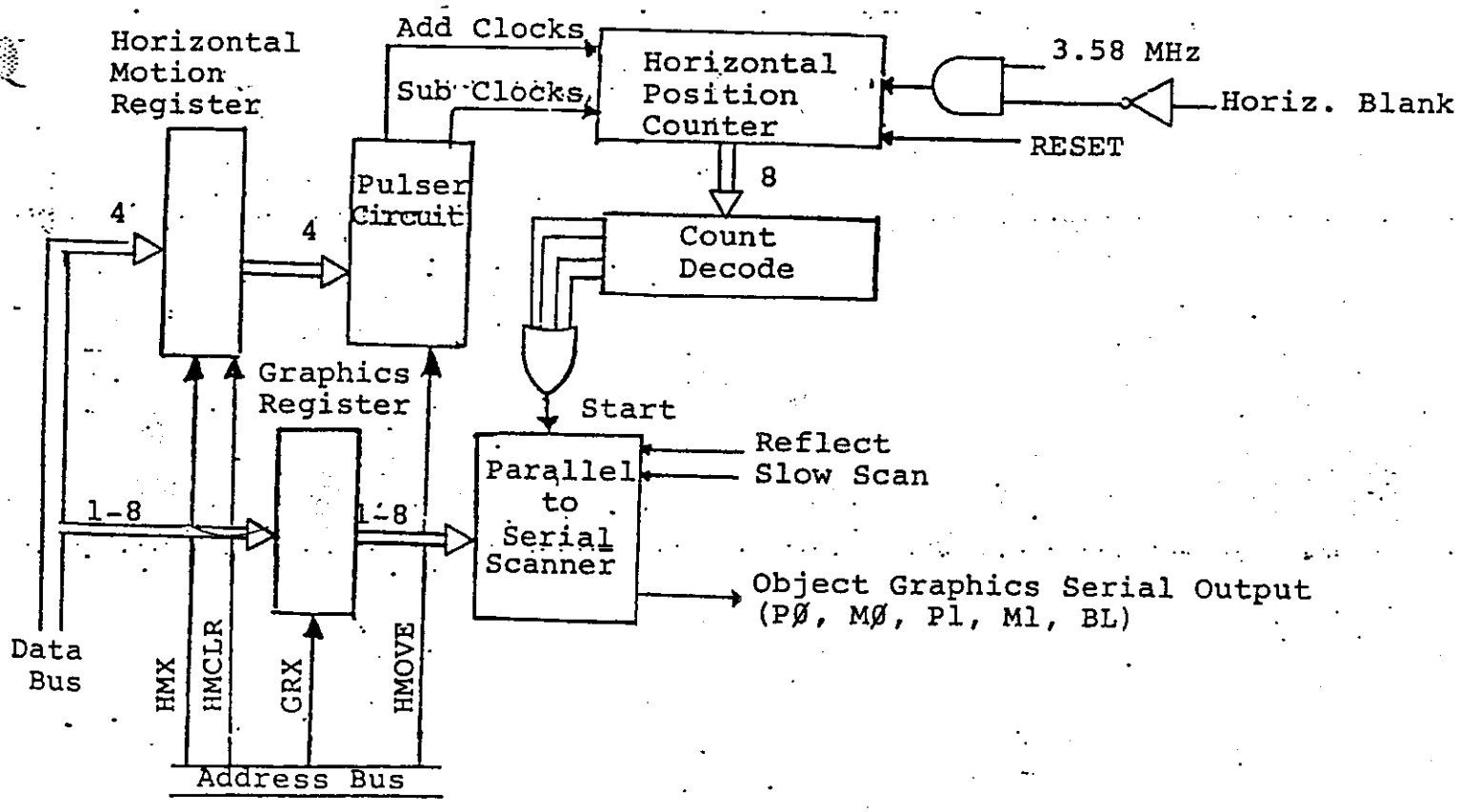


Figure 6. Horizontal Motion Circuit

6.3.6 OBJECT PRIORITIES

Simultaneous serial outputs from the graphics registers represent overlap on the television screen. In order to have color-luminosity values assigned to individual objects, it is necessary to establish priorities between objects when overlapped. The priority encoder (see Figure 10) produces 4 register select lines. These 4 lines select either background, player 0, player 1 or playfield. Only one of them can be true at a time.

6.3.6.1 Priority Assignment

Each object is assigned a priority so when any two objects overlap, the one with the highest priority will appear to move in front of the other. To simplify hardware logic, each missile is given the same color-lum value and priority as its corresponding player, and the ball is given the same color-lum value and priority as the playfield. The background has the lowest priority. The default priority assignments are as follows:

PRIORITY	OBJECTS
1 (highest)	P0, M0
2	P1, M1
3	B1, PF
4 (lowest)	BK

Objects with higher priority will appear to move in front of objects with lower priority. Players and missiles will move in front of the playfield.

6.3.6.2 Priority Control

There are two bits in the Playfield Control register (CTRLPF) that affect priority. Bit 2 of CTRLPF affects playfield priority (PFP) and bit 1 of CTRLPF affects score control.

6.3.6.2.1 When a "1" is written into the PFP bit, the priorities will be as follows:

PRIORITY	OBJECTS
1 (highest)	PF, BL
2	P0, M0
3	P1, M1
4 (lowest)	BK

Players and missiles will now move behind the playfield.

6.3.6.2.2 When a "1" is written into the score control bit, the score on the left half of the playfield gets the color of Player 0, and the score on the right half of the playfield gets the color of Player 1. When a "0" is written into the score control bit, the scores default to the color of the playfield.

3.7 COLLISION DETECTION

e serial outputs from all the graphics registers represent real time rizontal locations of objects on the television screen. If any of these tputs occur at the same time, they will overlap (collide) on the screen. llisions can occur between any of the 6 objects (playfield and 5 moveable jects). There are 15 possible two-object collisions which are stored in 15 e bit latches. See Section for collision combinations. Each collision gister contains two of these latches which are read by the processor on D6 d D7 of the data bus. A "1" on the data line indicates a collision has curred. The collision registers are usually read during vertical blank ter all possible collisions have occurred. Figure 7 below shows the llision detection circuit.

e collision registers are reset simultaneously by writing to the Collision set register (CXCLR). The reset is usually done near the end of vertical ank, after all collisions have been tested.

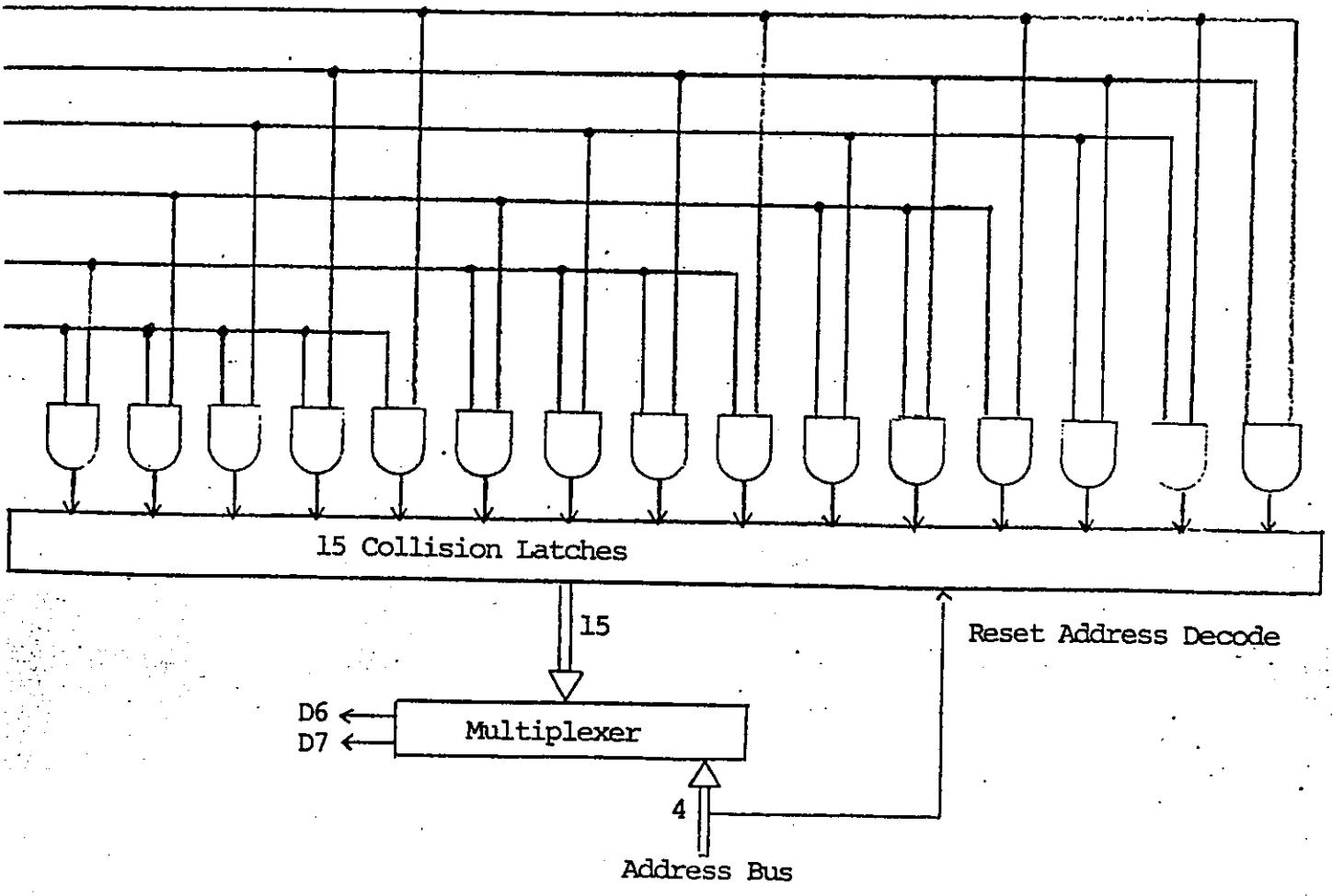


Figure 7. Collision Detection

6.3.8 INPUT PORTS

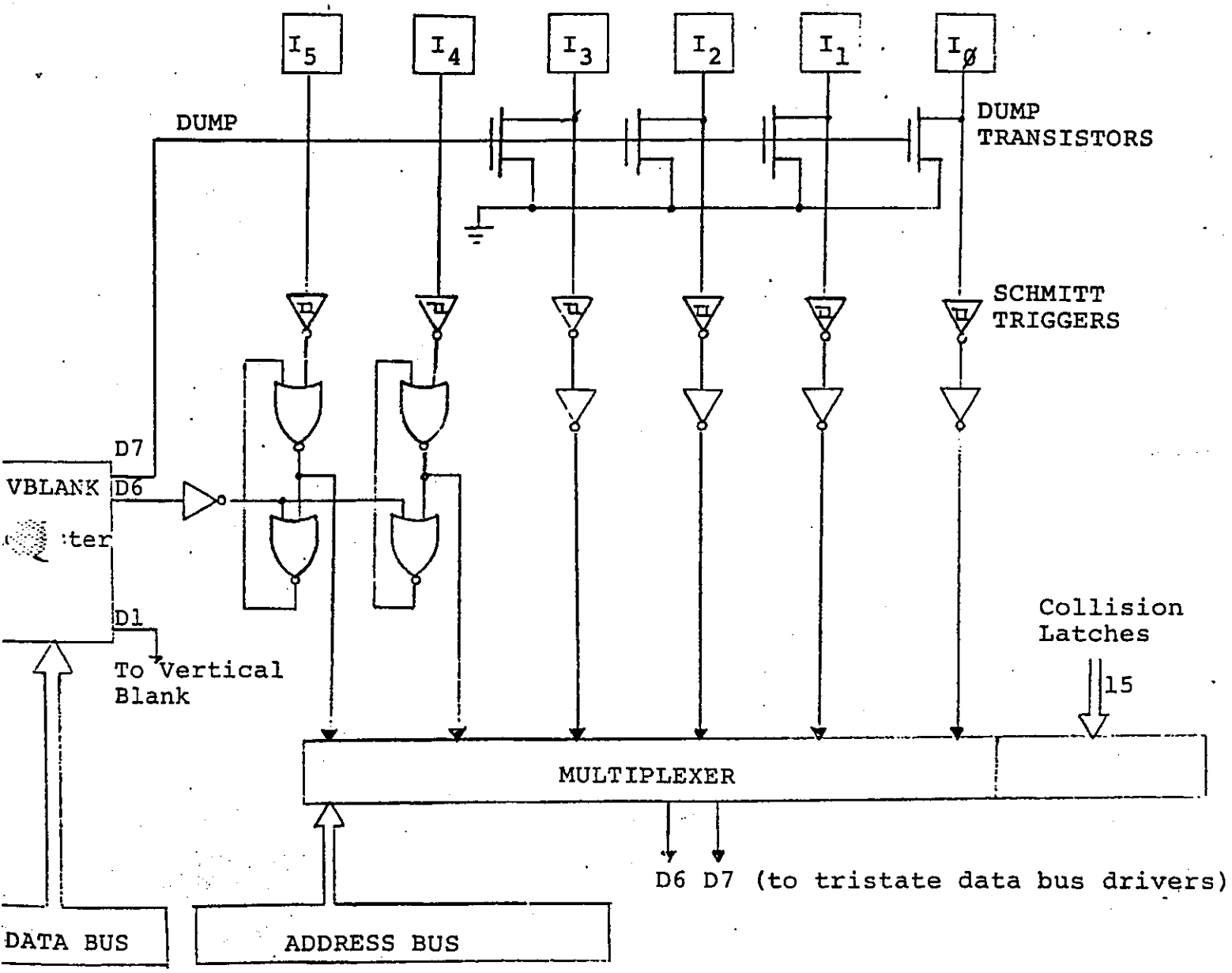
There are 6 input ports whose logic state may be read on data line 7 with read addresses INPT0 through INPT5. These 6 ports are divided into two types: dumped and latched. See Figure 8 for port circuitry.

6.3.8.1 Dumped Ports (I0-I3)

These 4 I/O ports are used in the 2100 and 2600 game systems to read 4 paddle positions from an external potentiometer-capacitor circuit controlled by the knob on the controller. The output of the pot is used to charge a capacitor in the console. When the capacitor is charged, the I/O port bit goes high. The processor discharges the capacitor by writing a logic one to D7 of VBLANK which grounds the input ports. When bit 7 of VBLANK is cleared, the potentiometers begin to recharge the capacitors. The microprocessor measures the amount of time it takes to detect a logic one at each port.

6.3.8.2 Latched Ports (I4-I5)

These two input ports are connected to the trigger buttons of the joystick controllers in the 2100 and 2600 game systems. They have latches that are both enabled or disabled by writing to D6 of VBLANK. Writing a '1' to D6 of VBLANK enables the latches and writing a '0' to D6 of VBLANK disables the latches. When the latches are disabled, the microprocessor reads the logic level of the port directly. When the latches are enabled, the processor reads the latches. When first enabled, the latch is set at a logic one. The latch remains at a logic one until its port goes low. When the port goes low, the latch is cleared and remains low regardless of what the port does.



INPUT PORTS

Figure 8.

6.3.9 AUDIO

There are two semi-independent audio channels which can be operated simultaneously to produce sound effects through the TV speaker. Each channel has its own frequency, noise and volume control, an 8 bit "divide by N" frequency divider, and an 8 bit control register (See Figure 9).

6.3.9.1 Frequency Select

Clock pulses at approximately 30 KHz from the horizontal sync counter pass through a "divide by N" circuit which is controlled by the output code from a five bit frequency register (AUDF0, AUDF1). When the processor writes to the frequency register, it causes the 30 KHz clocks to be divided by a selectable integer from 1 to 32 (see Section 7.7.2 for frequency values). Pulses are produced that are digitally adjustable from approximately 30 KHz to 1 KHz and are used to clock the noise-tone generator.

6.3.9.2 Noise-Tone Generator

The noise-tone generator is controlled by writing to the 4 bit audio control registers (AUDC0, AUDC1). The values written cause different sounds to be generated from pure tones to poly counter noise. There are three polynomial counters (9, 5, and 4 bit) used to generate random noise. Since the poly counters are sampled by the "divide by N" frequency divider, the output cannot change faster than the sampling rate. See Section 7.7.1 for audio control values.

6.3.9.3 Volume Select

The shift counter output is used to drive the audio output pad through four driver transistors that are graduated in size. Each transistor is twice as large as the previous one and is enabled by one bit from the audio volume register (AUDV0, AUDV1). As binary codes 0 through 15 are loaded by the processor, the pad drive transistors are enabled in a binary sequence. The shift counter output can pull down on the audio output pad with 16 selectable impedance levels. The volume selection is controlled by bits 0 through 3 of the Audio Volume Registers. The audio output of either channel can be completely turned off by writing zero to the volume control bits. All ones give maximum volume. See Section 7.7.3 for volume control values.

6.3.10 COLOR AND LUMINOSITY

Color and luminosity can be assigned to the Background, Playfield, Ball, Player 0, Player 1, Missile 0, and Missile 1. There are four color-lum registers of 7 bits each. The 4 most significant bits of the Color-Lum register will select one of 16 available colors. The remaining 3 bits select one of 8 levels of luminosity (brightness). See Section 7.8 for available colors and lums and Figure 10 for Color-Lum circuitry. The color-lum registers are set up as follows:

COLOR-LUM REGISTER	OBJECTS COLORED
COLUMP0	P0, M0
COLUMP1	P1, M1
COLUMPF	PF, BL
COLUMBK	BK

So, if the COLUMP1 register was set for green, both P1 and M1 would be drawn green.

The serial graphics outputs from all 6 objects are examined by the priority encoder which activates one of four select lines into a 4 X 7 multiplexer. This multiplexer then selects one of four color-lum registers as a 7 line output. The 3 binary coded luminosity lines and the internal sync line are fed into a D/A converter. The analog output goes directly to the composite video output pad. The 4 color lines go to the color phase shifter. The output of the color phase shifter goes to the chroma output pad.

The color phase shifter produces a reference color output (color burst) during horizontal blank. Then during the unblanked portion of the line it produces a color output shifted in phase with respect to the color burst. The amount of phase shift determines the color and is selected by the four color code lines from the color-lum multiplexer. Code 0 selects no color. Code 1 selects light orange (same phase as color burst). Codes 2 through 15 shift the phase from zero through almost 360 degrees allowing selection of 15 colors. Each phase shift is approximately 20 ns from the reference color output. Two phase shifts would have a delay of approximately 40 ns.

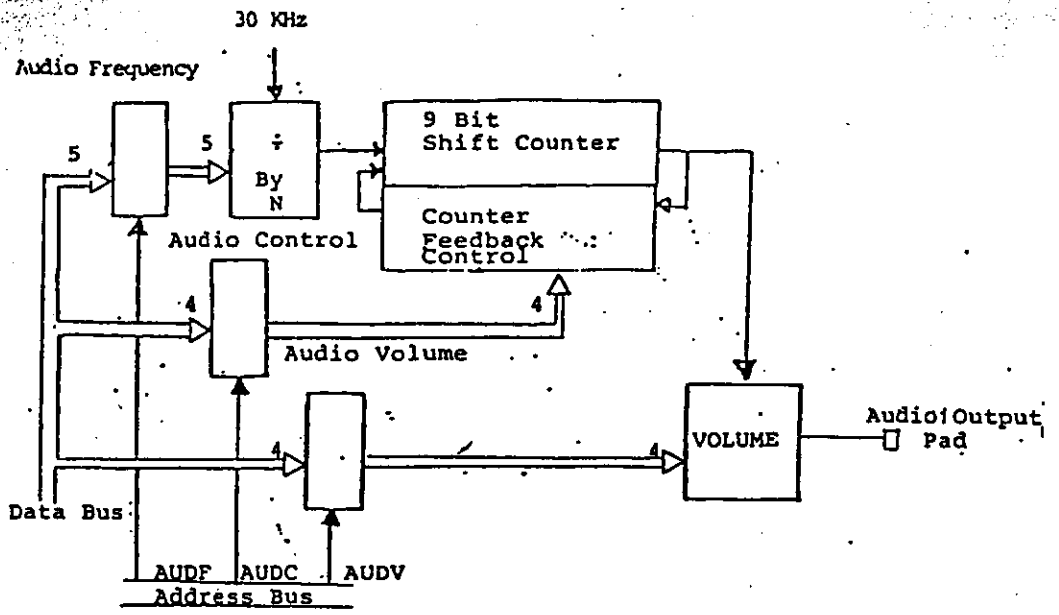


Figure 9 . Audio Circuit

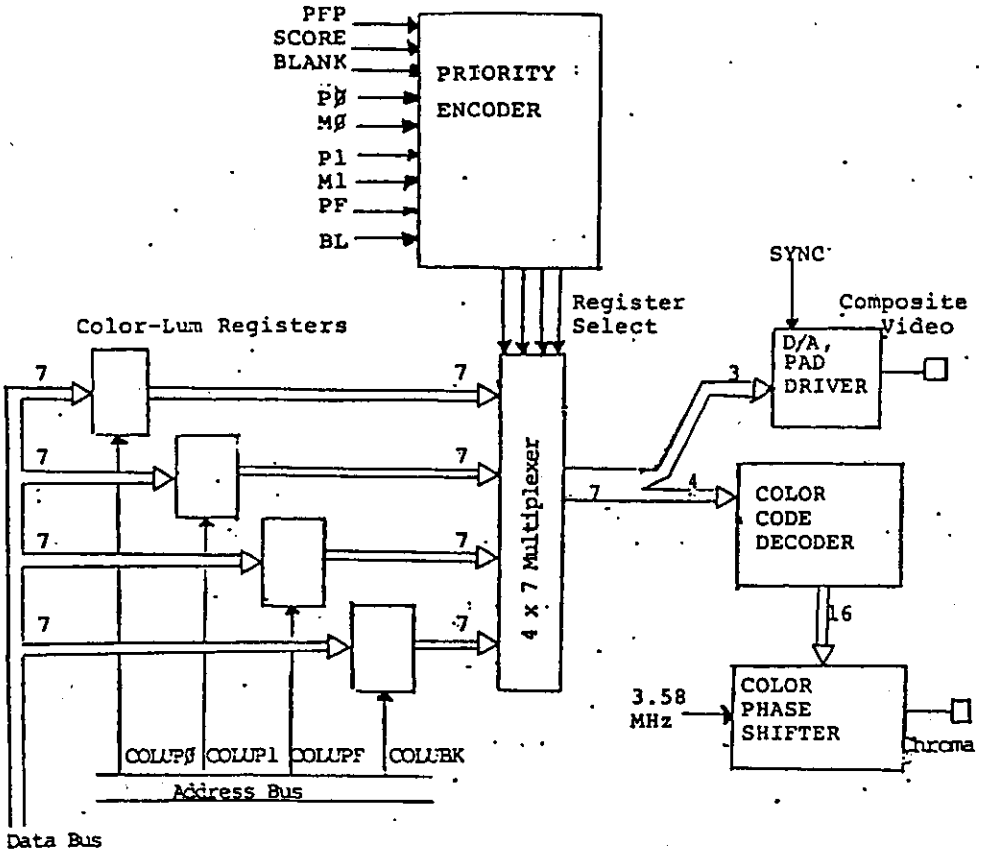


Figure10 . Color-Luminance

7.1 Vertical Timing Registers:

7	6	5	4	3	2	1	ø	
X	X	X	X	X	X	Start/ Stop VSYNC	X	VSYNC
IØ-I3 Ports	I4-I5 Latches	X	X	X	X	Start/ Stop VBLANK	X	VBLANK

7.1.1 Bit 1 of the VSYNC register controls the start and stop of the vertical sync time.

Bit 1 = '1' start vertical sync
= 'Ø' stop vertical sync

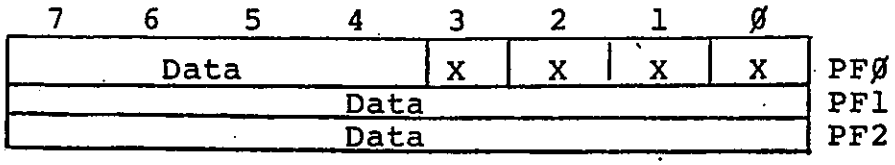
7.1.2 The VBLANK register contains the controls for the vertical blank and the latches and dumping transistors on input ports IØ - I5.

Bit 1 = '1' Start vertical blank
= 'Ø' Stop vertical blank

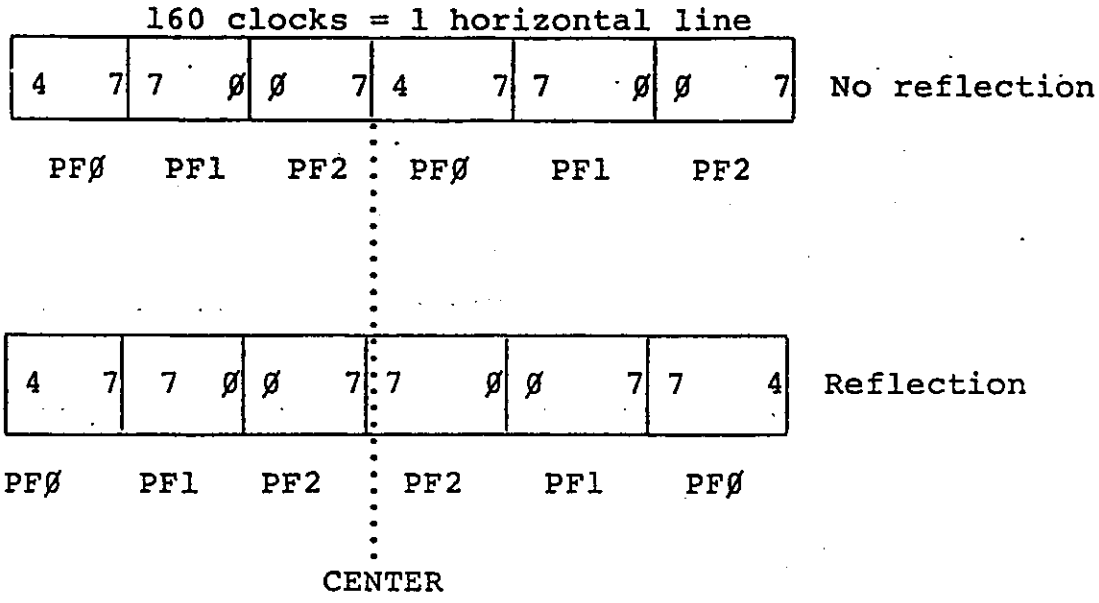
Bit 6 = '1' Enable I4, I5 latches
= 'Ø Disable I4, I5 latches

Bit 7 = '1' Dump IØ-I3 ports to ground
= 'Ø' Remove path to ground

7.2 Playfield Graphics Register:



The 20 bit serial output playfield register consists of 3 registers: PFØ (4 MSB), PF1 (8 bits), and PF2 (8 bits) and looks as follows on the television display:



One bit = 4 clocks

7.3 Playfield Control Register (CTRLPF)

7	6	5	4	3	2	1	Ø
X	X	Ball Size		X	PFP	Score	Ref

The CTRLPF register controls the reflection, score, and priority of the playfield and the ball size.

Ball Size:

Bits 5	4	Width
0	0	1 clock
0	1	2 clocks
1	0	4 clocks
1	1	8 clocks

PFP (playfield priority): Bit 2 = '1' Playfield has priority over players (players move behind playfield).

Bit 2 = '0' Players have priority over playfield.

Score: Bit 1 = '1' Score on left half of playfield gets color of player Ø and score on right half of playfield gets color of player 1.

Bit 1 = '0' Score defaults to color of playfield

Ref (reflect playfield): Bit Ø = '1' playfield reflected

Bit Ø = 'Ø' playfield not reflected

4 Moving Object Graphics Registers:

7	6	5	4	3	2	1	Ø	
X	X	X	X	X	X	Disable/ Enable Missile Ø	X	ENAMØ
X	X	X	X	X	X	Disable/ Enable Missile 1	X	ENAM1
X	X	X	X	X	X	Disable/ Enable Ball		ENABL
X	X	Clock width		X	Player-Missile Ø number & Player Size			NUSIZØ
X	X	Clock width		X	Player-Missile 1 number & Player Size			NUSIZ1
Player 1 Graphics Data								GRPØ
Player 2 Graphics Data								GRP1
X	X	X	X	Reflect PlayerØ	X	X	X	REFPØ
X	X	X	X	Reflect Player1	X	X	X	REFP1
X	X	X	X	X	X	X	Vertical Delay Player Ø	VDELPØ
X	X	X	X	X	X	X	Vertical Delay Player 1	VDELP1
X	X	X	X	X	X	X	Vertical Delay Ball	VDELBL

7.4.1 Enable Registers:

Bit 1 of the ENAMØ, ENAM1, and ENABL registers enables or disables missile Ø, missile 1 or the ball.

Bit 1 = '1' enables object
= 'Ø' disables object

7.4.2 Number and Size Registers:

Bits 5-4 of the NUSIZØ and NUSIZ1 registers control the clock width of the missiles.

D5	D4	Width
0	0	1 clock
0	1	2 clocks
1	0	4 clocks
1	1	8 clocks

.5 Horizontal Position Reset

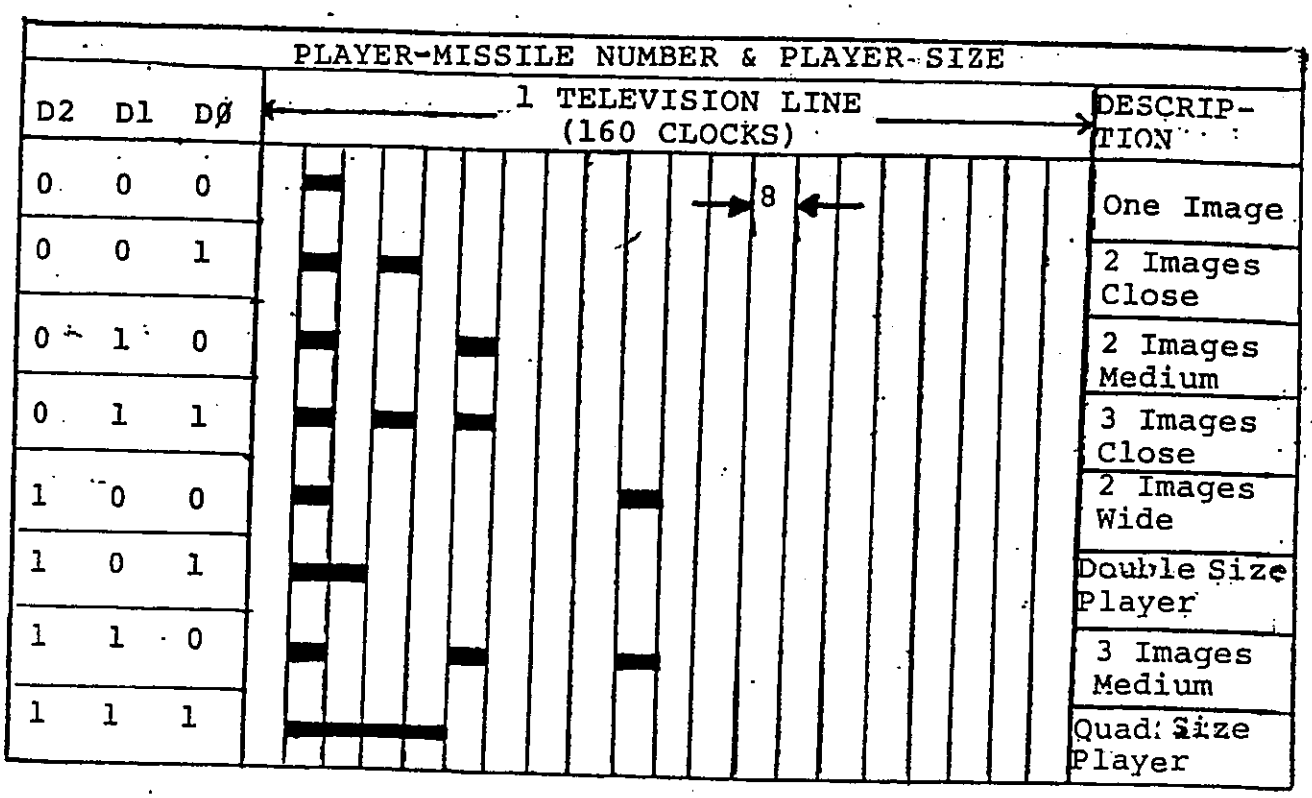
X	X	X	X	X	X	Reset Missile/ Player Ø	X	RESMP Ø
X	X	X	X	X	X	Reset Missile/ Player 1	X	RESMP 1

The RESMPØ and RESMP1 registers reset the horizontal location of a missile to the center of the corresponding player.

Bit 1 = '1' The missile remains locked to the center of it's player. The missile graphics are disabled.

Bit 1 = 'Ø' The missile graphics are enabled and can be moved independently from the player

Bits 2-Ø of NUSIZØ and NUSIZ1 control the number of images per player-missile and the player size.



4.3 Graphics Registers: Bits 7-Ø of the GRPØ and GRP1 registers contain the player Ø and 1 graphics data which are output serially. When reflected, bit Ø becomes the most significant bit and bit 7 the least significant bit.

4.4 Reflect Registers: Bit 3 of the REFPØ and REFP1 registers when enabled can reflect the player Ø and player 1 8-bit graphics data.

Bit 3 = 'Ø' no reflection (D7 = MSB)
= '1' reflect (DØ = MSB)

4.5 Vertical Delay Registers: Bit Ø of the VDELPØ, VDELP1, and VDELBL registers when enabled delays the players or the ball by one vertical line.

Bit Ø = 'Ø' no delay
= '1' delay

5 Horizontal Motion Registers

7	6	5	4	3	2	1	Ø	
Player Ø horizontal motion				X	X	X	X	HMPØ
Player 1 horizontal motion				X	X	X	X	HMP1
Missile Ø horizontal motion				X	X	X	X	HMMØ
Missile 1 horizontal motion				X	X	X	X	HMM1
Ball horizontal motion				X	X	X	X	HMBL

These registers will cause horizontal motion of the players, missiles and ball when the HMOVE command is executed. These registers should not be modified during the 24 computer cycles immediately following the HMOVE command as unpredictable motion values may result.

Bit 7	6	5	4	Motion	
0	1	1	1	+7	
0	1	1	0	+6	
0	1	0	1	+5	move left indicated
0	1	0	0	+4	# of clocks
0	0	1	1	+3	
0	0	1	0	+2	
0	0	0	1	+1	
0	0	0	0	No motion	
1	1	1	1	-1	
1	1	1	0	-2	
1	1	0	1	-3	move right indicated
1	1	0	0	-4	# of clocks
1	0	1	1	-5	
1	0	1	0	-6	
1	0	0	1	-7	
1	0	0	0	-8	

7.7 Audio Registers

7	6	5	4	3	2	1	Ø	
X	X	X	X	Audio Control Ø				AUDCØ
X	X	X	X	Audio Control 1				AUDC1
X	X	X	Audio Frequency Ø					AUDFØ
X	X	X	Audio Frequency 1					AUDF1
X	X	X	X	Audio Volume Ø				AUDVØ
X	X	X	X	Audio Volume 1				AUDV1

7.7.1 The 4 least significant bits of the audio control registers (AUDCØ, AUDC1) control the noise-tone generation circuit. A variety of noise and pure tones can be generated by either dividing the clock pulses from the divide by N circuit (pure tones) or by using a 4, 5, or 9 bit poly counter (random noise). See figure

Bit 3	2	1	Ø	Noise type or clock division
0	0	0	0	set 4 LSB of shift counter = 1 (no sound)
0	0	0	1	4 bit poly
0	0	1	0	4 bit poly ÷ 15
0	0	1	1	4 bit poly shifted into 5 bit poly
0	1	0	0	÷ 2 clock
0	1	0	1	÷ 2 clock
0	1	1	0	÷ 31 clock
0	1	1	1	5 bit poly ÷ 2
1	0	0	0	9 bit poly (white noise)
1	0	0	1	5 bit poly
1	0	1	0	÷ 31 clock
1	0	1	1	set 4 LSB of shift counter = 1 (no sound)
1	1	0	0	÷ 6 clock
1	1	0	1	÷ 6 clock
1	1	1	0	÷ 93 clock
1	1	1	1	5 bit poly ÷ 6

7.7.2 The 5 least significant bits of the Audio Frequency Divider registers (AUDFØ, AUDF1) can be selected to divide the 30KHZ clock by the integers from 1 to 32. See figure

Bit 4	3	2	1	Ø	Divisor
0	0	0	0	0	no division (÷1)
0	0	0	0	1	÷2
0	0	0	1	0	÷3
		⋮			⋮
1	1	1	1	0	÷31
1	1	1	1	1	÷32

.3 The 4 least significant bits of the Audio Volume registers (AUDVØ, AUDV1) determine the pull down impedance driving the audio output pads. See figure .

Bit 3	2	1	Ø	Audio Output Pulldown Current
0	0	0	0	No output current
0	0	0	1	Lowest
	⋮			⋮
1	1	1	0	
1	1	1	1	Highest

7.8 COLOR LUMINANCE REGISTERS

7	6	5	4	3	2	1	0	
Color					Lum		X	COLUP0
Color					Lum		X	COLUP1
Color					Lum		X	COLUPF
Color					Lum		X	COLUBK

The 7 most significant bits of the Color-Luminance registers determine the color (bits 7 through 4) and luminance (bits 3 through 1) of the players, playfield and background.

D7	D6	D5	D4	Color Range (dependent on Luminance value)
0	0	0	0	Gray
0	0	0	1	Light Orange
0	0	1	0	Orange
0	0	1	1	Reddish orange
0	1	0	0	Pink
0	1	0	1	Purple
0	1	1	0	Purple- Blue
0	1	1	1	Blue
1	0	0	0	Blue
1	0	0	1	Light Blue
1	0	1	0	Turquoise
1	0	1	1	Blue-Green
1	1	0	0	Green
1	1	0	1	Greenish Yellow
1	1	1	0	Gold
1	1	1	1	Light Orange

D3	D2	D1	Luminance
0	0	0	Dark
0	0	1	.
0	1	0	.
0	1	1	.
1	0	0	Grey
1	0	1	.
1	1	0	.
1	1	1	Light

Strobed Addresses

WSYNC (Wait for Sync):

This address halts the microprocessor by clearing RDY latch (Logic '0'). RDY is set true again by the leading edge of horizontal blank.

RSYNC (Reset Sync):

This address resets the horizontal sync counter to define the beginning of the horizontal blank time. It is used in chip testing.

RESPØ, RESP1, RESMØ, RESM1, RESBL (Reset Players, Missiles, and Ball):

These 5 addresses reset the players, missiles, and the ball. The object will begin its horizontal line serial graphics at the time the reset occurs.

HMOVE (horizontal motion):

This address implements the horizontal motion register values. The HMOVE strobe must occur at the beginning of the horizontal blank time in order to allow time for generation of extra clock pulses into the horizontal position counters. If motion is desired, HMOVE must immediately follow a WSYNC command in the program.

HMCLR (horizontal motion clear)

This address clears all horizontal motion registers to zero (no motion).

CXCLR (collision Reset):

This address clears all collision latches to zero (no collisions).

7.10 READ ADDRESSES

7.10.1 Read Collisions

	7	6	5	4	3	2	1	0	
00 CXM0P	M0*P1	M0*P0	X	X	X	X	X	X	Missile 0 Collision
01 CXM1P	M1*P0	M1*P1	X	X	X	X	X	X	Missile 1 Collision
02 CXP0FB	P0*PF	P0*BL	X	X	X	X	X	X	Player 0 Collision
03 CXP1FB	P1*PF	P1*BL	X	X	X	X	X	X	Player 1 Collision
04 CXM0FB	M0*PF	M0*BL	X	X	X	X	X	X	Missile 0 Collision
05 CXM1FB	M1*PF	M1*BL	X	X	X	X	X	X	Missile 1 Collision
06 CXBLPF	BL*PF	X	X	X	X	X	X	X	Ball Collision
07 CXPPMM	P0*P1	M0*M1	X	X	X	X	X	X	Player/Missile Collision

7.10.2 Read Input Ports

08 INPT0	I0	X	X	X	X	X	X	X	Pot Port I0
09 INPT1	I1	X	X	X	X	X	X	X	Pot Port I1
0A INPT2	I2	X	X	X	X	X	X	X	Pot Port I2
0B INPT3	I3	X	X	X	X	X	X	X	Pot Port I3
0C INPT4	I4	X	X	X	X	X	X	X	Input Port I4
0D INPT5	I5	X	X	X	X	X	X	X	Input Port I5

X = don't care

The leftmost column contains the 6 bit hex address of the particular read command. The address is followed by the assigned address name.

8. MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	-55 to +150°C
Ambient Temperature	0 to +70°C
Voltage at any Pin Relative to Vss	-0.3 to 7.0V
Power Dissipation	1.0 W

9. CAPACITANCES

Ambient Temperature Parameters: T_A = 25°C, V_{cc} = 5V ± 5%, GND = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
C_{in}	Input Capacitance		10	pF	
C_{out}	Output Capacitance		12	pF	
$C_{I/O}$	I/O Capacitance		15	pF	
C_{OSC}	OSC Capacitance		15	pF	
C_{inp}	PA-PB Input Capacitance		10	pF	
C_{outp}	PA-PB Output Capacitance		10	pF	

10. D.C. CHARACTERISTICS

Ambient Temperature Parameters: T_A = 0 to 70°C; V_{cc} = +5V ± 5%

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{IH}	Input High Current PA,PB ports	-100		uA	V_{in} = 2.4V
I_{IL}	Input Low Current PA,PB ports		-1.6	mA	V_{in} = 0.4V
I_{OL}	Output Low Current PA,PB ports	1.6		mA	V_{OL} = 0.4V
I_{OH}	Output High Current PA,PB ports	-100		uA	V_{OH} = 2.4V
V_{IH}	Input High Voltage			V	
	$\overline{OSC}$	2.4			
	$\overline{RES}$	3.0			
	I0-I3	2.6			
	I4-I5	4.75			
	All other inputs	2.0			
V_{IL}	Input Low Voltage			V	
	OSC	-0.3	0.4		
	$\overline{I0-I3}$		1.0		
	$\overline{RES}$		0.6		
	All other inputs		0.8		
I_{IN}	Input Leakage Current		10	uA	V_{in} = 0 to 5.25V V_{cc} = 5.0V
	$\overline{RES}$		2.5		
	OSC		10		
I_{TSI}	3-state Input Current		10	uA	V_{in} = 0.4 to 2.4V V_{cc} = 5.25V
V_{OH}	Output High Voltage			V	
	Logic, PA-PB ports	2.4			I_{load} = 100uA
	Comp. Video, Chroma	2.8			V_{cc} = 4.75V
	Audio (OFF)	3.7			

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OL}	Output Low Voltage			V	
	Logic, PA-PB ports, Comp. Video, Chroma		0.4		I_{load} = 1.6 mA V_{cc} = 4.75V
	Audio				
	10/10 on		3.7		10K pullup
	20/10 on		2.9		@ V_{cc} = 4.6V
	40/10 on		1.8		
	80/10 on		1.2		
I_{cc}	Maximum V_{cc} Current		190	mA	

11. A.C. CHARACTERISTICS

11.1 Television Interface

Number	Symbol	Parameter	Min	Max	Unit	Comments
1	T_{tads}	Address, R/W, chip select set up time		230	ns	
2	t_{Tadh}	Address, R/W, chip select hold time	10		ns	
3	t_{Tds}	Data Stability Time		200	ns	
4	t_{Tdh}	Data Hold Time	10		ns	
5	t_{Tdso}	D7-D6 Stability Time		170	ns	
6	t_{Tdho}	D7-D6 Hold Time	60		ns	
7	t_{ninv}	Color Delay Line Output (see Table 2).		190	ns	Open Drain, Pull up resistor effects leading edge delay.
8	t_{rlh}	Falling edge of OSC to rising edge of RDY		390	ns	
9	t_{rhl}	Falling edge of OSC to falling edge of RDY		260	ns	
10	t_{sync}	Falling edge of OSC to rising edge of $\overline{SYNC}$		530	ns	
11	t_{lum}	Lum and blank data valid after falling edge of OSC		250	ns	
12	t_{col}	COL data valid after rising edge of OSC		360	ns	

11.2 Clocks

13	t_{opw}	OSC pulse width	120	160	ns
14	t_{orf}	OSC rise and fall time		20	ns
15	t_{oh}	OSC falling edge to 0_o rising edge time		240	ns
16	t_{ol}	OSC rising edge to 0_o falling edge time		170	ns

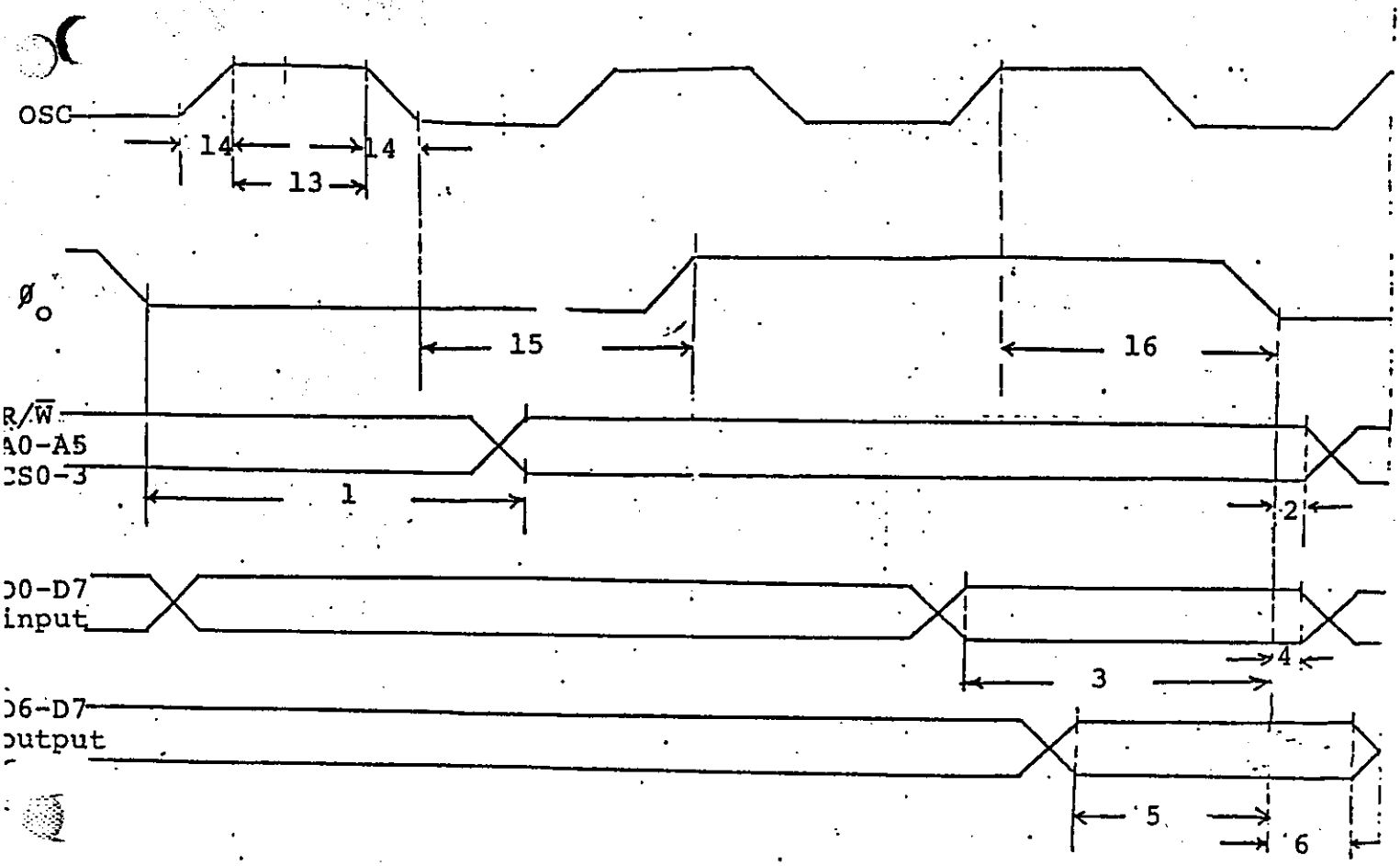
11.3 COMBO Timing

17	t_{cyc}	0_o Cycle Time	0.8	100	us
18	t_{rf0o}	0_o Rise, Fall Time		10	ns
19	t_{pw0o}	0_o Pulse Width	375	62000	ns
20	t_{rws}	R/W Setup Time		280	ns
21	t_{ads2}	Address Set up Time		280	ns
22	t_{dsu2}	Data Stability	110		ns
23	t_{hr}	Data Hold Time-Read	130		ns
24	t_{cdr}	Data Valid Delay-Read Timer or RAM		370	ns
25	t_{mds}	Data Set up Time		240	ns
26	t_{rdy}	Ready Set up Time	130		ns
27	t_{cpw}	Peripheral Data Valid after Falling Edge of 0_o (writing)		0.8	us
28	t_{pcr}	Peripheral Data Valid Before Rising Edge of 0_o (reading)	240		ns

11.4 Color Delay Times

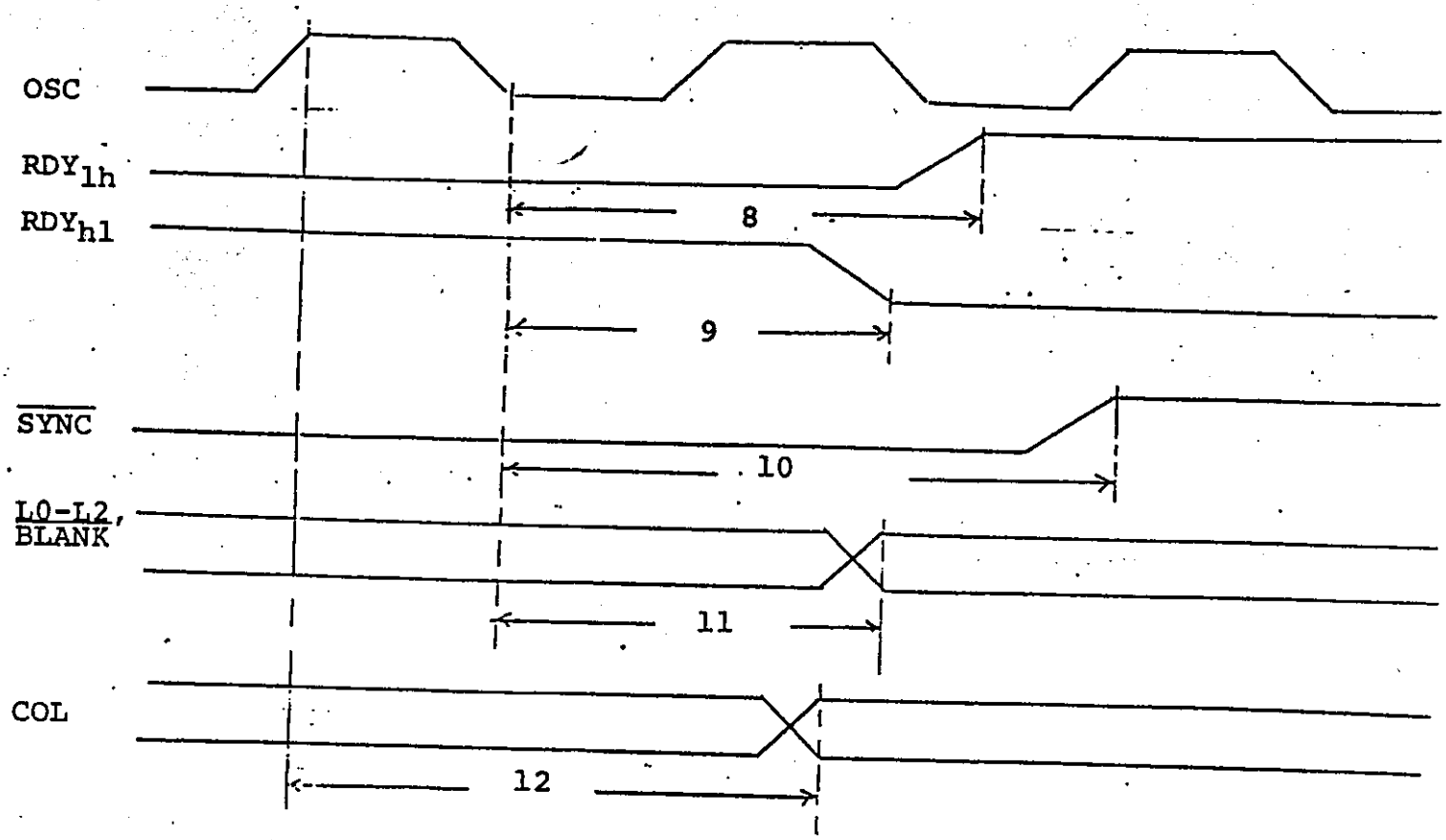
COLOR VALUE (HEX)	DELAY TIME FOR COLOR VALUE
0	NO COLOR OUT
1	$t_{ninv} + 0\Delta t$
2	$t_{ninv} + 1\Delta t$
3	$t_{ninv} + 2\Delta t$
4	$t_{ninv} + 3\Delta t$
5	$t_{ninv} + 4\Delta t$
6	$t_{ninv} + 5\Delta t$
7	$t_{ninv} + 6\Delta t$
8	$t_{ninv} + 7\Delta t$
9	$t_{ninv} + 8\Delta t$
A	$t_{ninv} + 9\Delta t$
B	$t_{ninv} + 10\Delta t$
C	$t_{ninv} + 11\Delta t$
D	$t_{ninv} + 12\Delta t$
E	$t_{ninv} + 13\Delta t$
F	$t_{ninv} + 14\Delta t$

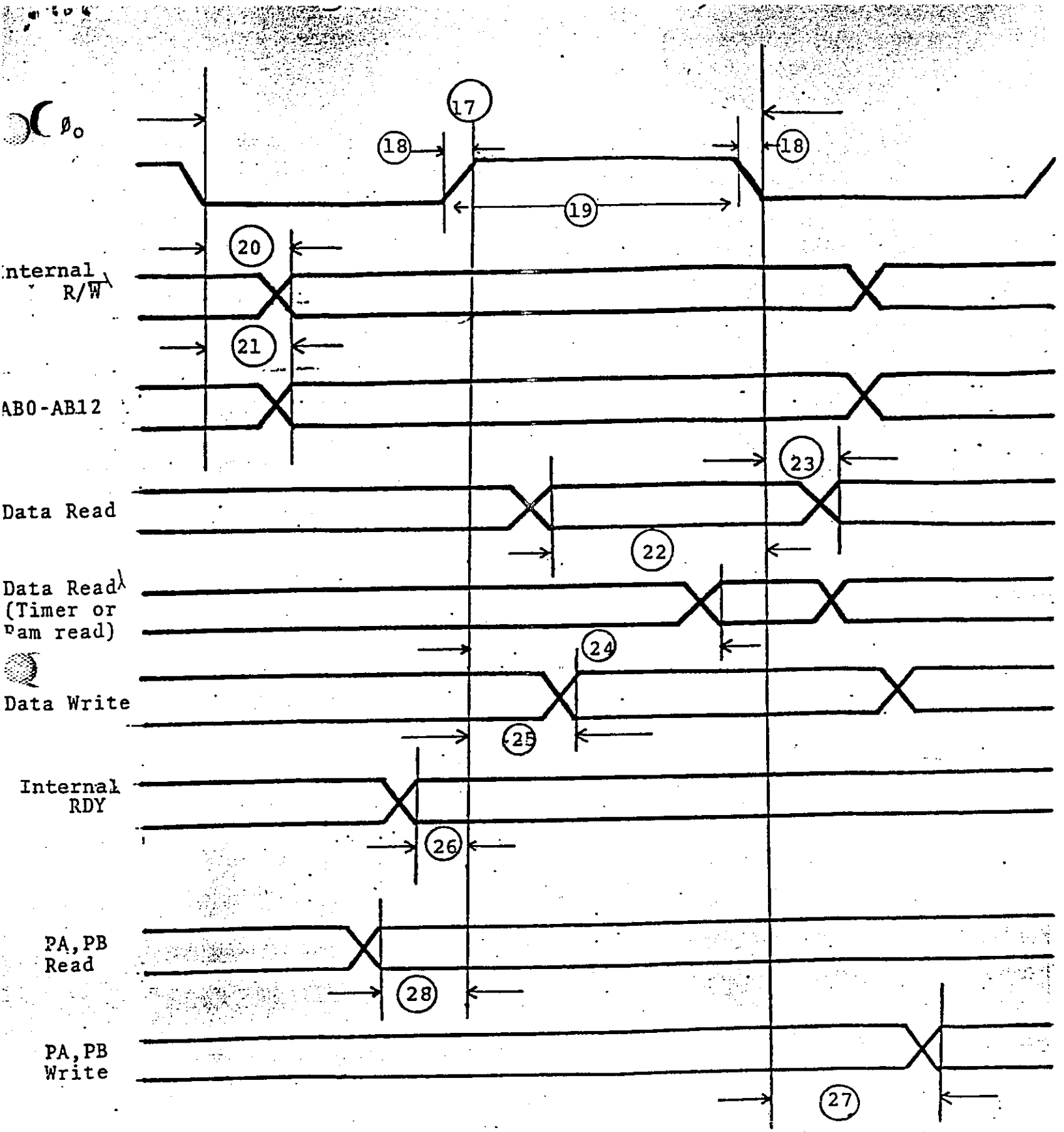
Table 2. Delay Times for Color Values (CHROMA).



ϕ_o = the output clock on All during the Stephanie test

Television Interface





ϕ_o = the input clock at the I2 pin during the COMBO test